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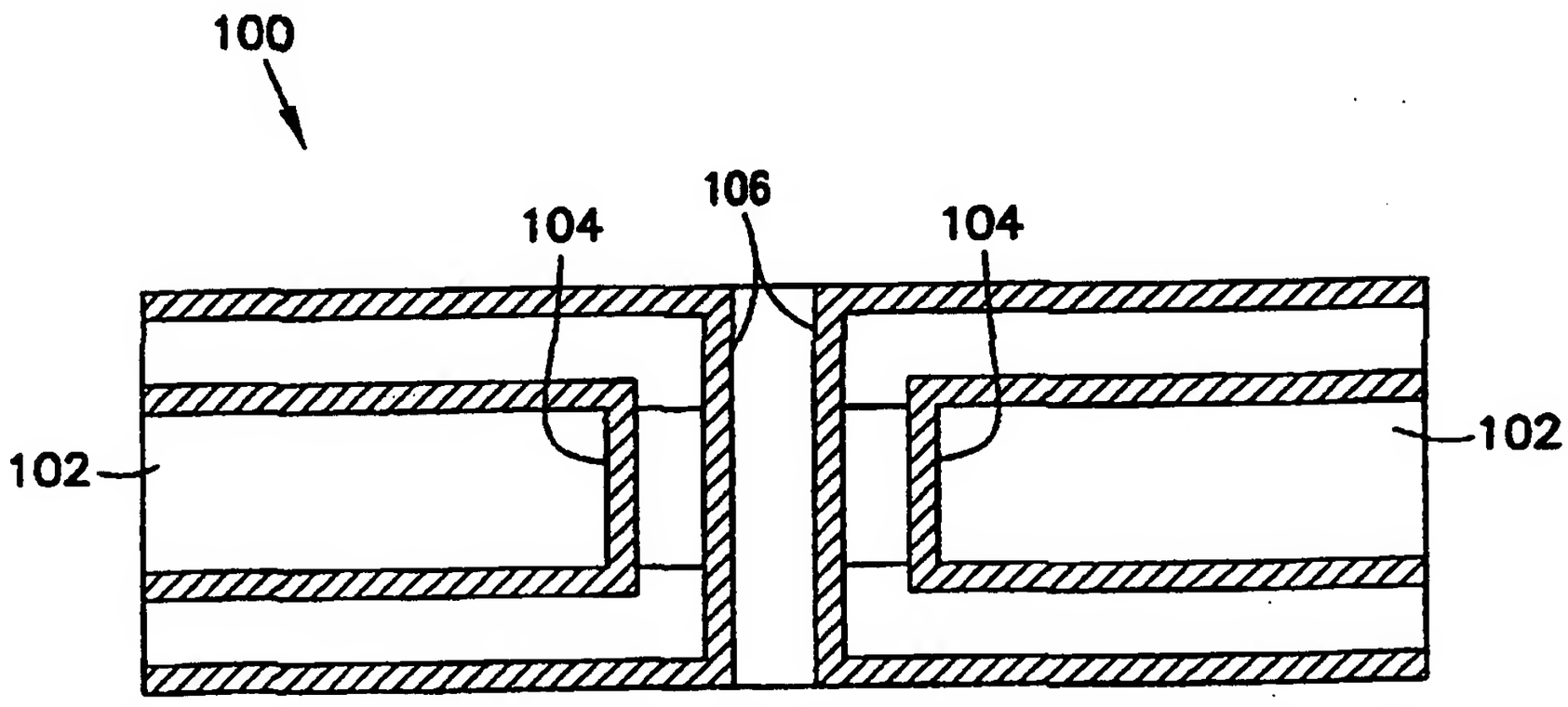
(54) Title: INTERCONNECT STRUCTURE AND METHOD OF FABRICATION THEREFOR



(57) Abstract: An interconnect structure for microelectronic devices includes a first plated through hole (PTH) via formed through a core material, and a second PTH via concentrically located inside first PTH via, but electrically isolated from the first PTH via. A method of producing the interconnect structure includes forming a first hole through a core material layer, then forming a first conductive layer on sidewalls of the first hole, and on upper and lower surfaces of the core material layer. The first hole is substantially filled with non-conductive material, and dielectric layers are formed on substantially horizontal portions of the first conductive layer, and on top and bottom surfaces of the non-conductive material. A second hole, having a smaller diameter than the diameter of the first hole, is formed through the dielectric layers and the non-conductive material in concentric relationship to the first hole. A second conductive layer is then formed on the sidewalls of the second hole, and on upper and lower surfaces of the dielectric layers.

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Interconnect Structure and Method of Fabrication Therefor

Technical Field of the Invention

The present invention relates generally to microelectronic structures and fabrication methods, and more particularly to interconnect structures and methods of fabricating the same.

Background of the Invention

Advances in semiconductor manufacturing technology have led to the development of integrated circuits having multiple levels of interconnect. In such an integrated circuit, patterned conductive material on one interconnect level is electrically insulated from patterned conductive material on another interconnect level by films of material such as silicon dioxide or organic polymers. Connections between the conductive material at the various interconnect levels are made by forming openings in the insulating layers and providing an electrically conductive structure such that the patterned conductive material from different interconnect levels are brought into electrical contact with each other. These structures are often referred to as contacts, vias or interconnect structures.

The power supplied to a chip through an organic package must travel through a core layer by way of plated through hole (PTH) vias, where the core layer is a solid internal layer in the printed circuit board stackup. Unfortunately, the PTH via is a relatively high inductance feature, due to the relatively large distance between the PTH via and its ground potential reference along a vertical axis.

Figure 1 is a representation of an electrical circuit 10 that simulates the effective power supply inductance, L_{eff}. This schematic applies in the context of very high frequency switching. The circuit includes a capacitor 12 connected to the V_{CC} and V_{SS} pads on an integrated circuit chip. An inductor 14, 18 and a resistor 16, 20 are present on both the supply and return paths from the capacitor 12.

The effective power supply inductance, L_{eff}, is related to the number, N, of PTH vias by the equation:

$$L_{eff} = \frac{1}{\sum_{N} \frac{1}{L_{PTH}}}$$

where L_{PTH} is the inductance of a PTH via.

Since all PTH vias associated with a single package typically have the same inductance, the effective power supply inductance contribution from the package is:

$$L_{eff} = \frac{L_{PTH}}{N}$$

Thus, the effective power supply inductance is inversely proportional to the number of PTH vias. Because of this relationship, one common prior art method for reducing power supply inductance involves placing extra PTH vias in the package. This has the effect of reducing the value of inductors 14, 18 (Figure 1). Essentially, each signal-carrying via is surrounded by vias that carry the ground. In some cases, the vias are arranged in a face-centered square configuration, where the central dot would represent the power supply via, and the four outer dots would represent the ground-carrying vias.

Unfortunately, the practice of adding PTH vias solely for the purpose of reducing power supply inductance results in larger package designs and/or more complicated fabrication techniques. These results occur because the additional vias consume more area on the package, and many more vias must be drilled during the fabrication process than are necessary to carry data signals alone.

Besides having inductance problems relating to the power supply, the characteristics of prior art PTH vias also result in electrical signal integrity problems. Transient signals traveling through a package either from or to a chip must travel through the PTH vias. When these signals travel through the PTH vias, they lose the controlled ground or power reference plane they had when propagating along traces in the package. This loss of controlled ground and shielding results in signal integrity problems which can result in overshoot, undershoot, ringback, and/or crosstalk.

For the reasons stated above and for other reasons stated below, which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an interconnect structure design and method of fabrication that results in reduced inductance of the power supply to a chip attached to an organic package. In addition, there is a need for an interconnect structure design and method of fabrication therefor that allows signals traveling through the interconnect structure to maintain their shielding and reference, thus reducing signal integrity problems.

Summary of the Invention

In one embodiment, a method for fabricating an interconnect structure involves forming a first PTH via through a core material, where the first PTH via is electrically connected to a first conductive material layer. Then, a second PTH via is formed so that it is concentrically located inside the first PTH via. The second PTH via has a diameter that is smaller than a diameter of the first PTH via, and the second PTH via is electrically isolated from the first PTH via and electrically connected to a second conductive material layer.

The interconnect structure includes the first PTH via formed through the core material, where the first PTH via is electrically connected to the first conductive material layer. The structure also includes the second PTH via concentrically located inside the first PTH via, where the second PTH via has a

diameter that is smaller than a diameter of the first PTH via. In addition, the second PTH via is electrically isolated from the first PTH via and electrically connected to the second conductive material layer.

Brief Description of the Drawing

Figure 1 is a representation of an electrical circuit that simulates the effective power supply inductance;

Figure 2 is a schematic cross-section of an interconnect structure in accordance with one embodiment of the present invention;

Figure 3 illustrates a flowchart of a method for fabricating an interconnect structure in accordance with one embodiment of the present invention;

Figures 4-11 are schematic cross-sections illustrating various stages of fabrication of an interconnect structure in accordance with one embodiment of the present invention;

Figure 12 illustrates an example of an integrated circuit housed by a package having via structures in accordance with one embodiment of the present invention; and

Figure 13 illustrates a general purpose computer system that includes a printed circuit board having a microprocessor housed by a package having via structures in accordance with one embodiment of the present invention.

Detailed Description of the Invention

The terms "chip," "integrated circuit," "monolithic device," "semiconductor device," and "microelectronic device" are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The term "via" commonly refers to structures for electrical connection of conductors from different interconnect levels. This term is sometimes used in the art to describe both an opening in an insulator in which an interconnect structure will be completed, and the completed structure itself. For purposes of this disclosure, "via" refers to the opening and "interconnect structure" refers to the completed structure itself.

The term "horizontal," as used herein, means substantially parallel to the surface of a substrate, and the term "vertical," as used herein, means substantially orthogonal to the surface of a substrate.

In order to manufacture integrated circuits with reduced inductance of the power supply to a chip attached to an organic package, it is desirable to produce interconnect structures that have the ground potential reference closer to the power supply source. In addition, it is desirable to produce interconnect structures that allow signals to maintain their reference when traveling through the interconnect structure, thus reducing signal integrity problems such as overshoot, undershoot, ringback and crosstalk. As will be described below, embodiments of the present invention both reduce inductance of the power supply and allow signals to better maintain their shielding and reference, thus improving signal integrity.

Figure 2 is a schematic cross-section of an interconnect structure 100 in accordance with one embodiment of the present invention. Essentially, interconnect structure 100 includes a first PTH via 104 formed through a core material 102, and a second PTH via 106 concentrically located inside the first PTH via 104, but electrically isolated from the first PTH via 104.

Figure 3 illustrates a flowchart of a method for fabricating the interconnect structure shown in Figure 1 in accordance with one embodiment of the present invention. In order to best describe the method of fabricating, Figure 3 should be viewed in conjunction with Figures 4-11, which include schematic cross-sections illustrating various stages of fabrication of an interconnect structure in accordance with one embodiment of the present invention.

The method begins, in block 202, by providing a core material layer 102 (FIG. 4), which has an upper surface 304 and a lower surface 306. In one embodiment, core material layer 102 is an organic substrate, such as an epoxy material. For example, standard printed circuit board materials such as FR-4, BT, Teflon, other epoxy resins, or the like could be used in various embodiments. Both the upper and lower surfaces 304, 306 of core material layer 102 are substantially horizontal. In various embodiments, the thickness of core material layer 102 is within a range of 600-1000 microns, with it being

approximately 800 microns in one embodiment. Core material layer 102 could be thicker or thinner than this range in other embodiments.

In block 204, a first hole 402 (FIG. 5) is formed through the core material layer 102. In various embodiments, the diameter of first hole 402 is within a range of 200-500 microns, with it being approximately 350 microns in one embodiment. The diameter could be larger or smaller than this range in other embodiments. First hole 402 is defined by first sidewalls 404, which are substantially vertical, or orthogonal, to the upper and lower surfaces 304, 306 of core material layer 102. In one embodiment, the hole is mechanically drilled, although the hole may also be drilled using a laser or other drilling technologies in various other embodiments.

Next, in block 206, a first conductive layer 502 (FIG. 6) is formed on the first sidewalls 404 of the first hole 402, and on upper and lower surfaces 304, 306 of core material layer 102. In one embodiment, first conductive layer 502 is a copper layer, although other conductive metals or materials could be used in other embodiments. A first PTH via is defined by portions 104 of the first conductive layer 502 that are disposed on first sidewalls 404. Other portions 506 of the first conductive layer are horizontally-disposed on the upper and lower surfaces 304, 306 of core material layer 102, resulting in an electrical connection between the first PTH via 104 and the horizontally disposed portions 506 of the first conductive layer. In various embodiments, the thickness of first conductive layer 502 is within a range of 5-15 microns, with it being approximately 10 microns in one embodiment. First conductive layer 502 could be thicker or thinner than this range in other embodiments.

In block 208, the first hole 402 is substantially filled with non-conductive material 602 (FIG. 7). First hole 402 could be screen-filled, for example, with the non-conductive material 602. In one embodiment, non-conductive material 602 is an epoxy fill material, although other non-conductive materials also could be used in other embodiments. Non-conductive material 602 has a top surface 604 and a bottom surface 606, where the top surface 604 is substantially parallel to the upper surface 304 of core material 102, and the bottom surface 606 is substantially parallel to the lower surface 306 of core material 102.

In block 210, dielectric layers 702, 704 (FIG. 8) are formed on the substantially horizontal portions 506 of the first conductive layer 502, and on the top and bottom surfaces 604, 606 of the non-conductive material 602. In one embodiment, these dielectric layers 114, 116 are made of a non-conductive material that is the same as, or similar to the material used for core layer 102 or non-conductive material 602, although different dielectric materials could be used in other embodiments. In various embodiments, the thickness of dielectric layers 702, 704 is within a range of 20-40 microns, with it being approximately 30 microns in one embodiment. Dielectric layers 702, 704 could be thicker or thinner than this range in other embodiments.

The flowchart of Figure 2 shows first hole 402 being filled in block 208, and dielectric layers 702, 704 being applied in block 210. In an alternate embodiment, in block 210, the dielectric layers' non-conductive material could be allowed to flow into first hole 402 in order to fill first hole 402 with non-conductive material. In this embodiment, it would not be necessary to perform block 208.

Next, in block 212, a second hole 802 (FIG. 9) is formed within the filled first hole through the dielectric layers 702, 704 and non-conductive material 602. Second hole 802 can be formed in the same or a different manner as first hole 402. The second hole 802 has a diameter 804 that is smaller than a diameter 806 of the first PTH via 104. In various embodiments, the diameter of second hole 802 is within a range of 100-200 microns, with it being approximately 150 microns in one embodiment. This diameter could be larger or smaller than this range in other embodiments.

In one embodiment, the second hole 802 is concentrically located within the first PTH via 104. In other embodiments, the second hole 802 could be slightly off center with respect to the first PTH via 104. Thus, the use of the term "concentric" is intended to mean that the second hole exists within the first PTH via, not necessarily that the second hole is located exactly at the center of the first PTH via. The second hole is defined by second sidewalls 808, which are substantially vertical to the upper and lower surfaces 304, 306 of core material 102.

Then, in block 214, a second conductive layer 902 (FIG. 10) is formed on the second sidewalls 808 of second hole 802, and on upper and lower surfaces 904, 906 of dielectric layers 702, 704. Second conductive layer 902 could be made of the same or a different material as first conductive layer 502. In various embodiments, the thickness of second conductive layer 902 is within a range of 5-15 microns, with it being approximately 10 microns in one embodiment. Second conductive layer 902 could be thicker or thinner than this range in other embodiments.

A second PTH via is defined by portions 106 of the second conductive layer 902 that are disposed on second sidewalls 808. Other portions 910 of the second conductive layer are horizontally-disposed on the upper and lower surfaces 904, 906 of dielectric layers 702, 704, resulting in an electrical connection between the second PTH via 106 and the horizontally disposed portions 910 of the second conductive layer.

The second hole is located in such a manner that second conductive layer 902 does not come into contact with first conductive layer 502. Thus, the second PTH via 106 is electrically isolated from the first PTH via 104.

After formation of the interconnect structure as described in blocks 202-214, second hole 802 is filled with a non-conductive material 1002 (Figure 11) in block 216. Second hole 802 could be screen-filled, for example, or a next dielectric layer could be allowed to flow into second hole 802. After filling second hole 802, the method ends. The package can then be completed by adding one or more new conductive and non-conductive layers.

Figure 12 illustrates an integrated circuit 1102 housed by a package 1104 having interconnect structures in accordance with one embodiment of the present invention. The integrated circuit is located on a top surface 1106 of the package 1104, and contains a circuit which is electrically connected to one or more interconnect structures within the package. In one embodiment of the present invention, integrated circuit 1102 is an microprocessor, although integrated circuit 1102 could be other devices in other embodiments. A single interconnect structure or a series of interconnect structures within package 1104 provide an electrical path between the top surface 1106 and the bottom surface 1108 of package 1104.

Package 1104 has a plurality of connectors 1110 affixed to the bottom surface 1108. These connectors 1106 form contacts with metal pads (not shown) on a printed circuit (PC) board 1112, and thereby couple the package 1104 to the PC board 1112. Connectors 1110 could be, for example, solder balls that make contact with the PC board's metal pads, or the connectors could be pins that are insertable into sockets (not shown) on PC board 1112. In alternate embodiments, connectors 1110 could connect to one or more intermediate layers, rather than connecting directly to PC board 1112. For example, connectors 1110 could connect to an interposer (not shown) that acts as a dimensional interface between connectors 1110 and the metal pads on PC board 1112.

Figure 13 illustrates a general purpose computer system 1200 that includes a PC board 1202 having a microprocessor 1204 housed by a package 1206 having via structures in accordance with one embodiment of the present invention. Computer system 1200 is housed on PC board 1202, and includes bus 1208, microprocessor 1204, package 1206, power supply signal generator 1210, and memory 1212. Package 1206 couples micorprocessor 1204 to bus 1208 in order to communicate power supply signals and non-power supply signals between microprocessor 1204 and devices coupled to bus 1208. For the embodiment of the present invention shown in Figure 12, bus 1208 couples microprocessor 1204 to memory 1212 and power supply signal generator 1210. However, it is to be understood that in alternative embodiments of the present invention, microprocessor 1204 can be coupled to memory 1212 and power supply signal generator 1210 through two different busses. In addition, in alternative embodiments of the present invention, power supply signal generator 1210 is not positioned on PC board 1202, but instead is positioned elsewhere.

Thus, various embodiments of a PTH structure and methods of fabricating that structure have been described, along with a description of the incorporation of a package that includes that structure on a PC board within a general purpose computer system. Interconnect structures in accordance with the present invention both reduce inductance of the power supply and allow the signal integrity to be optimal by minimizing crosstalk and allowing signals to maintain their reference by providing a first PTH via formed through a core

material, and a second PTH via concentrically located inside first PTH via, but electrically isolated from the first PTH via. Referring to Figure 1, the embodiments of the present invention have the effect of further reducing the value of inductors 14, 18 than what is possible using prior art methods.

The first PTH via provides the ground and/or power plane, and also acts as a shielding conductor to contain the magnetic field produced by current through the second PTH via. The second PTH via acts as the current-carrying via, either for power supply or logic signals. Because the signals carried by the second PTH via are completely surrounded by the shielding conductor (i.e., the first PTH via), the second PTH via has low inductance characteristics, resulting in better signal quality. Also, additional PTH vias used solely for the purpose of bringing the ground potential reference closer to the signal via are unnecessary. Thus, the low-inductance interconnect structure of the present invention uses less package real estate than prior art packages that have the signal-carrying via surrounded by ground-carrying vias. In addition, the shielding characteristics of the interconnect structure result in improved signal quality.

Conclusion

Embodiments of the present invention provide an interconnect structure that includes a first PTH via formed through a core material, and a second PTH via concentrically located inside first PTH via, but electrically isolated from the first PTH via.

Embodiments of the present invention describe herein are beneficial in that inductance of the power supply to a chip attached to an organic package is substantially reduced. This is accomplished by placing the ground potential reference much closer to the power supply source. In addition, electrical signals maintain their reference and shielding while traveling through the interconnect structure, thus reducing signal integrity problems such as overshoot, undershoot, ringback, and crosstalk.

In the foregoing detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific preferred embodiments in

which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention.

It will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. For example, illustrative embodiments describe vias between two levels of interconnect. However, those skilled in the art will recognize that many interconnect levels may be connected by vias in accordance with the present invention.

This application is intended to cover any adaptations or variations of the present invention. The foregoing detailed description is, therefore, not to be taken in a limiting sense, and it will be readily understood by those skilled in the art that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated in order to explain the nature of this invention may be made without departing from the spirit and scope of the invention as expressed in the adjoining claims.

What is claimed is:

1. A method for forming an interconnect structure comprising:

forming a first plated through hole (PTH) via through a core material, wherein the first PTH via is electrically connected to a first conductive material layer; and

forming a second PTH via concentrically located inside the first PTH via, wherein the second PTH via has a diameter that is smaller than a diameter of the first PTH via, and the second PTH via is electrically isolated from the first PTH via and electrically connected to a second conductive material layer.

2. The method as claimed in claim 1, wherein forming the first PTH via comprises:

providing a core material layer having an upper surface and a lower surface, wherein the upper surface and the lower surface are substantially horizontal;

forming a first hole through the upper surface and the lower surface, wherein the first hole is defined by first sidewalls that are substantially vertical; and

forming a first conductive layer on the first sidewalls, the upper surface, and the lower surface.

3. The method as claimed in claim 2, wherein forming the second PTH via comprises:

substantially filling the first hole with a non-conductive material, wherein the non-conductive material has a top surface and a bottom surface, the top surface is substantially coplanar with the upper surface, and the bottom surface is substantially coplanar with the lower surface;

forming dielectric layers on substantially-horizontal portions of the first conductive layer, the top surface, and the bottom surface;

forming a second hole through the dielectric layers and the non-conductive material deposited in the first hole, wherein the second

hole is defined by second sidewalls that are substantially vertical and are formed of the non-conductive material; and

forming a second conductive layer on the second sidewalls.

4. The method as claimed in claim 2, wherein forming the second PTH via comprises:

forming dielectric layers of a non-conductive material on substantially-horizontal portions of the first conductive layer, wherein the non-conductive material flows into the first hole, substantially filling the first hole;

forming a second hole through the non-conductive material deposited in the first hole, wherein the second hole is defined by second sidewalls that are substantially vertical and are formed of the non-conductive material; and

forming a second conductive layer on the second sidewalls.

5. A method for forming an interconnect structure, comprising:

providing a core material layer having an upper surface and a lower surface, wherein the upper surface and the lower surface are substantially horizontal;

forming a first hole through the upper surface and the lower surface, wherein the first hole is defined by first sidewalls that are substantially vertical;

forming a first conductive layer on the first sidewalls, the upper surface, and the lower surface;

substantially filling the first hole with a non-conductive material, wherein the non-conductive material has a top surface and a bottom surface, the top surface is substantially coplanar with the upper surface, and the bottom surface is substantially coplanar with the lower surface;

forming dielectric layers on substantially-horizontal portions of the first conductive layer the top surface, and the bottom surface;

forming a second hole through the dielectric layers and the non-conductive material deposited in the first hole, wherein the second hole has a diameter that is smaller than a diameter of the first hole, and the second hole is

defined by second sidewalls that are substantially vertical and are formed of the non-conductive material; and

forming a second conductive layer on the second sidewalls.

6. The method as claimed in claim 5, further comprising substantially filling the second hole with a non-conductive material.

7. The method as claimed in claim 5, wherein providing a core material layer comprises providing an organic substrate.

8. The method as claimed in claim 7, wherein providing an organic substrate comprises providing an epoxy material.

9. The method as claimed in claim 5, wherein forming the first hole comprises mechanically drilling the first hole.

10. The method as claimed in claim 5, wherein forming the first hole comprises using a laser.

11. The method as claimed in claim 5, wherein substantially filling the first hole comprises filling the first hole with an epoxy fill material.

12. The method as claimed in claim 5, wherein forming the second hole comprises mechanically drilling the second hole.

13. The method as claimed in claim 5, wherein forming the second hole comprises using a laser.

14. An interconnect structure comprising:

a first plated through hole (PTH) via formed through a core material, wherein the first PTH via is electrically connected to a first conductive material layer; and

a second PTH via concentrically located inside the first PTH via, wherein the second PTH via has a diameter that is smaller than a diameter of the first PTH via, and the second PTH via is electrically isolated from the first PTH via and electrically connected to a second conductive material layer.

15. The interconnect structure as claimed in claim 14, further comprising a non-conductive material between the first conductive material layer and the second conductive material layer.

16. The interconnect structure as claimed in claim 14, wherein the core material is an organic substrate.

17. An interconnect structure comprising:
a core material layer having an upper surface and a lower surface, wherein the upper surface and the lower surface are substantially horizontal;
a first hole through the upper surface and the lower surface, wherein the first hole is defined by first sidewalls that are substantially vertical;
a first conductive layer formed on the first sidewalls, the upper surface, and the lower surface;
a non-conductive material that substantially fills the first hole, wherein the non-conductive material has a top surface and a bottom surface, the top surface is substantially coplanar with the upper surface, and the bottom surface is substantially coplanar with the lower surface;
dielectric layers formed on substantially-horizontal portions of the first conductive layer the top surface, and the bottom surface;
a second hole through the dielectric layers and the non-conductive material deposited in the first hole, wherein the second hole has a diameter that is smaller than a diameter of the first hole, and the second hole is defined by second sidewalls that are substantially vertical; and
a second conductive layer formed on the second sidewalls.

18. The interconnect structure as claimed in claim 17, wherein the core material layer comprises an organic substrate.

19. The interconnect structure as claimed in claim 18, wherein the organic substrate comprises an epoxy material.

20. The interconnect structure as claimed in claim 17, wherein the first conductive layer comprises an epoxy fill material.

21. An integrated circuit package comprising:

a package having one or more interconnect structures that provide electrical connections between a top surface of the package and a bottom surface of the package, wherein an interconnect structure includes a first plated through hole (PTH) via formed through a core material, and a second PTH via concentrically located inside the first PTH via, wherein the second PTH via has a diameter that is smaller than a diameter of the first PTH via, and the second PTH via is electrically isolated from the first PTH via; and

an integrated circuit located on the top surface of the package, the integrated circuit containing a circuit which is electrically connected to the interconnect structure.

22. The integrated circuit package as claimed in claim 21, wherein the integrated circuit is a microprocessor.

23. A computer system positioned on a printed circuit board, the computer system comprising:

a bus;

a memory coupled to the bus; and

an integrated circuit package including:

a package having one or more interconnect structures that provide electrical connections between a top surface of the package and a bottom surface of the package, wherein an interconnect structure includes a first plated through hole (PTH) via formed through a core material, and a second PTH via concentrically located inside the first PTH via,

wherein the second PTH via has a diameter that is smaller than a diameter of the first PTH via, and the second PTH via is electrically isolated from the first PTH via, and

a microprocessor located on the top surface of the package, the microprocessor containing a circuit which is electrically connected to the interconnect structure.

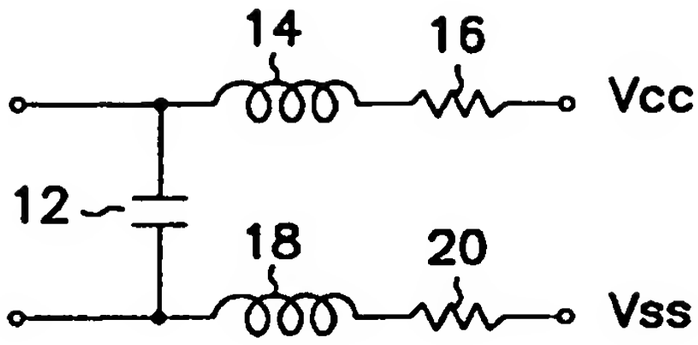

FIG. 1

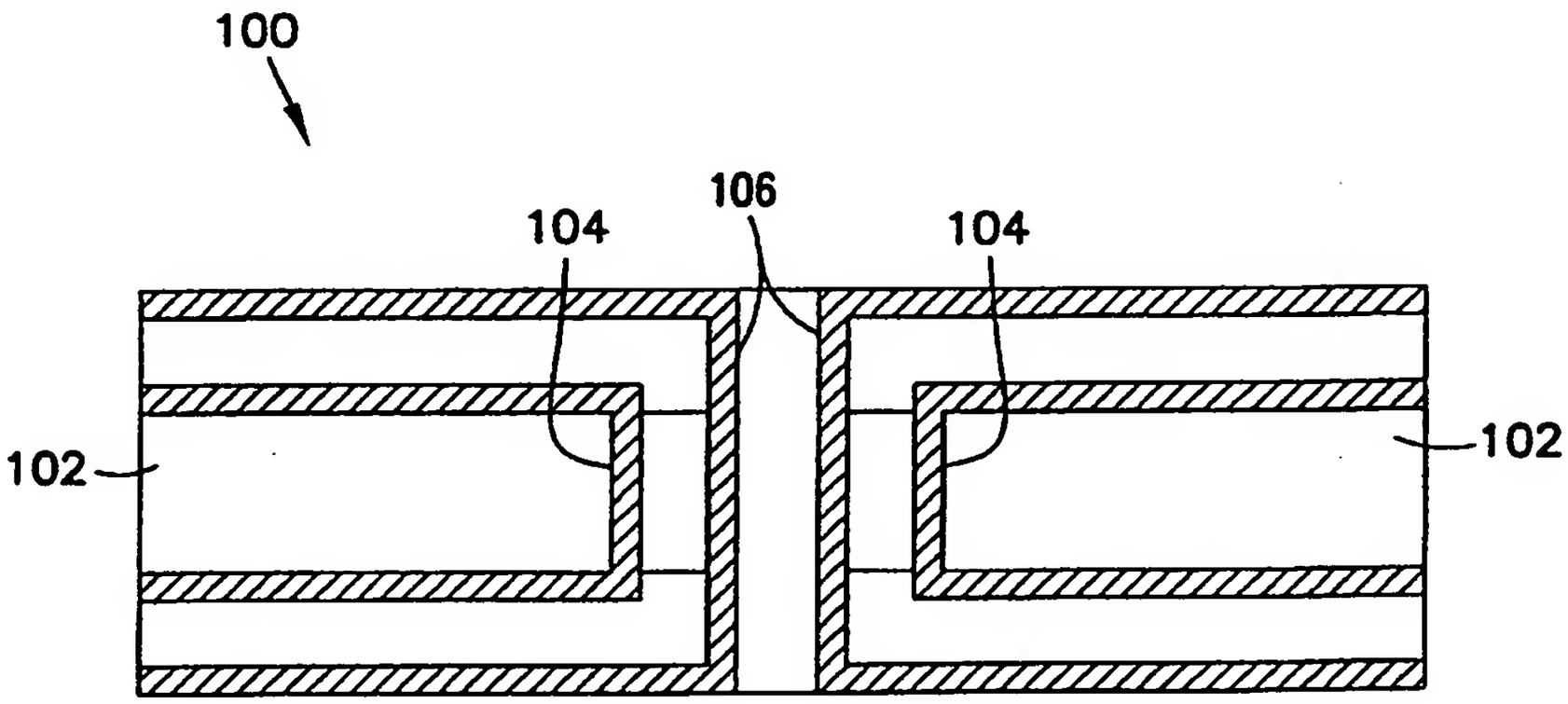

FIG. 2

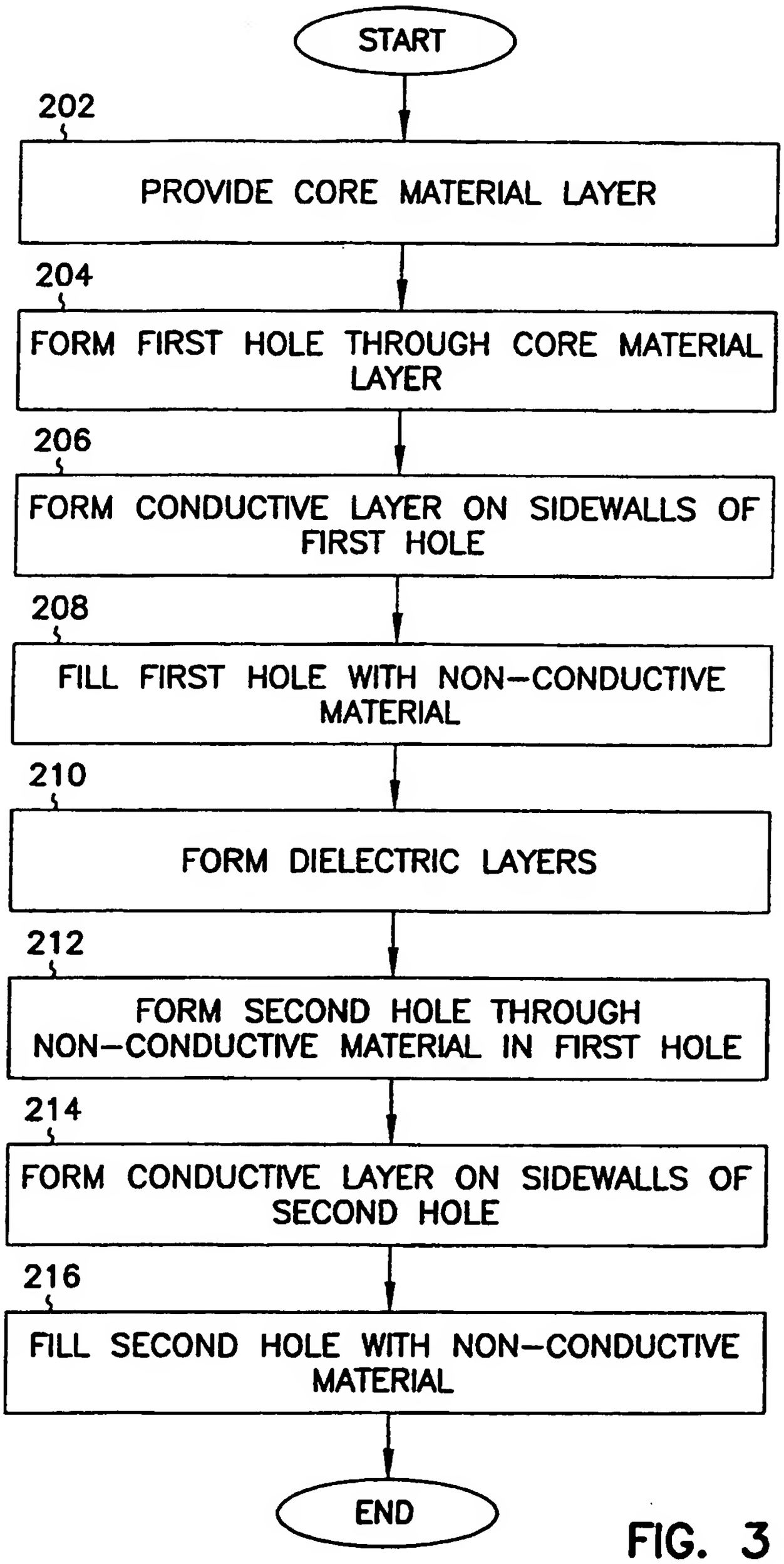
START
202
PROVIDE CORE MATERIAL LAYER
204
FORM FIRST HOLE THROUGH CORE MATERIAL LAYER
206
FORM CONDUCTIVE LAYER ON SIDEWALLS OF FIRST HOLE
208
FILL FIRST HOLE WITH NON-CONDUCTIVE MATERIAL
210
FORM DIELECTRIC LAYERS
212
FORM SECOND HOLE THROUGH NON-CONDUCTIVE MATERIAL IN FIRST HOLE
214
FORM CONDUCTIVE LAYER ON SIDEWALLS OF SECOND HOLE
216
FILL SECOND HOLE WITH NON-CONDUCTIVE MATERIAL
END

FIG. 3

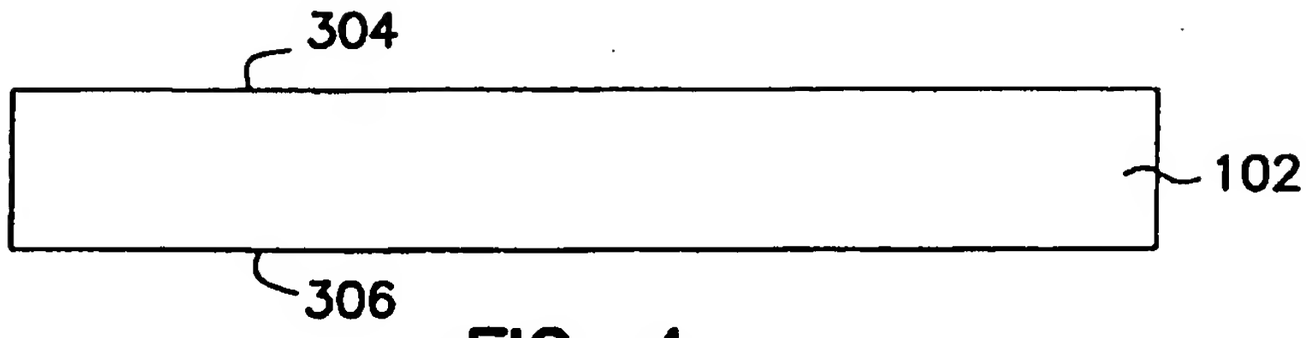

FIG. 4

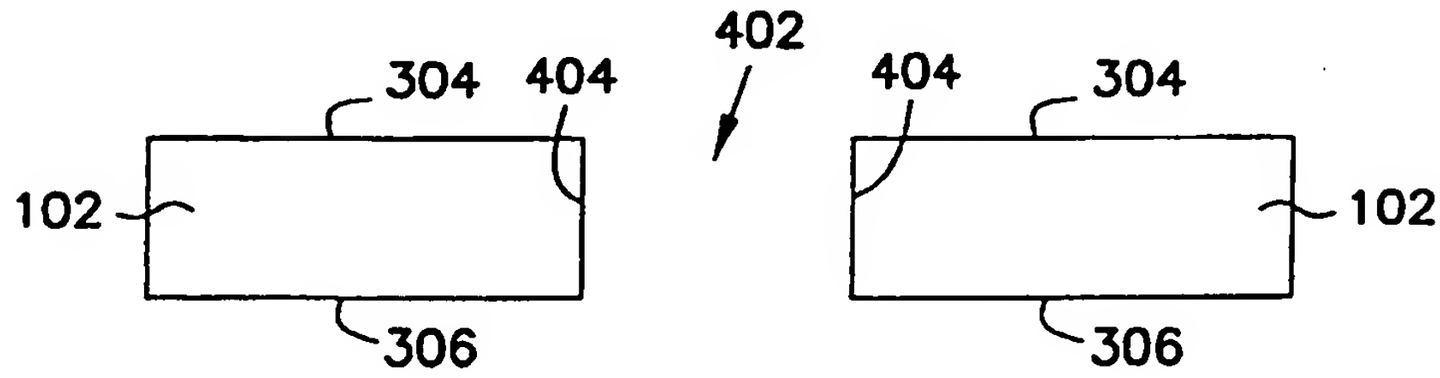

FIG. 5

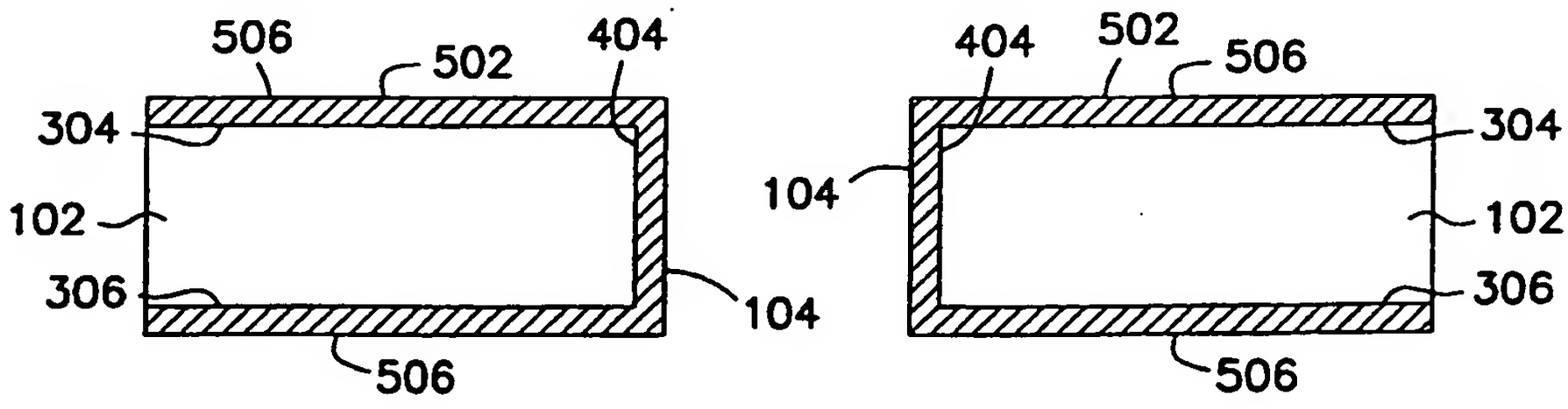

FIG. 6

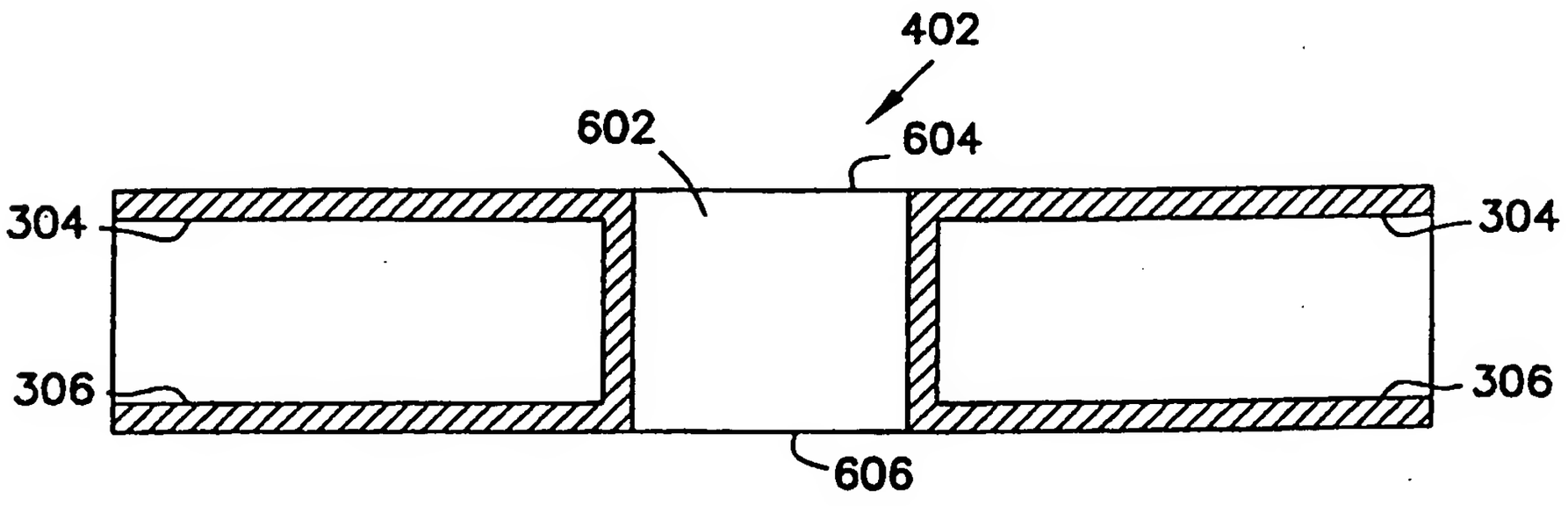

FIG. 7

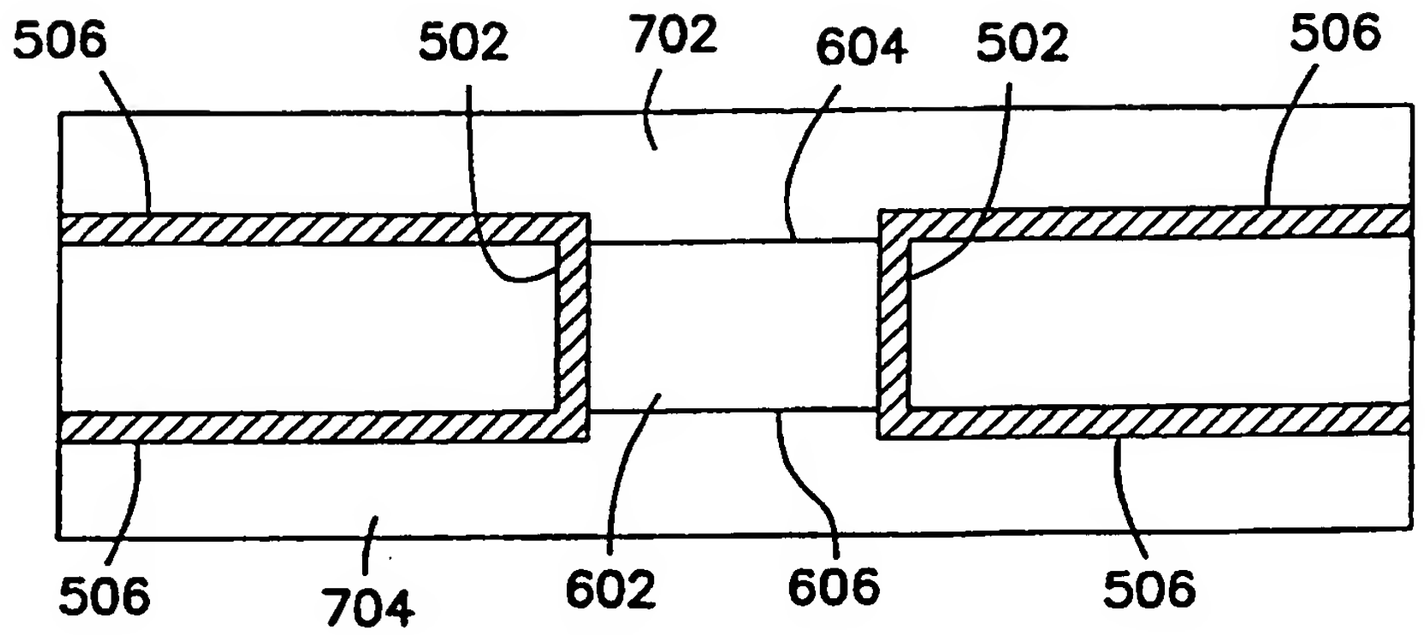
506
502
702
604
502
506
506
704
602
606
506

FIG. 8

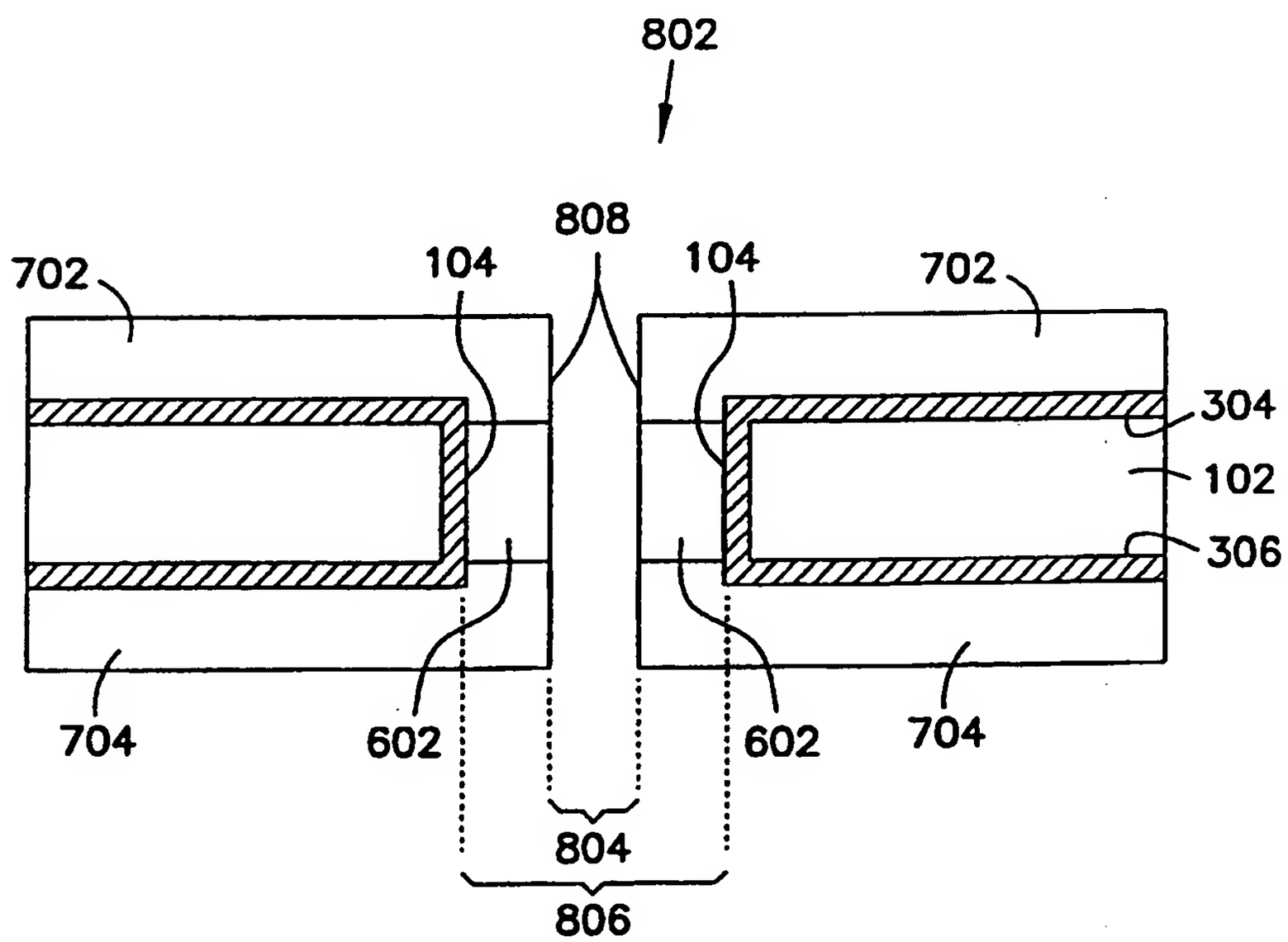
802
808
702
104
104
702
304
102
306
704
602
602
704
804
806

FIG. 9

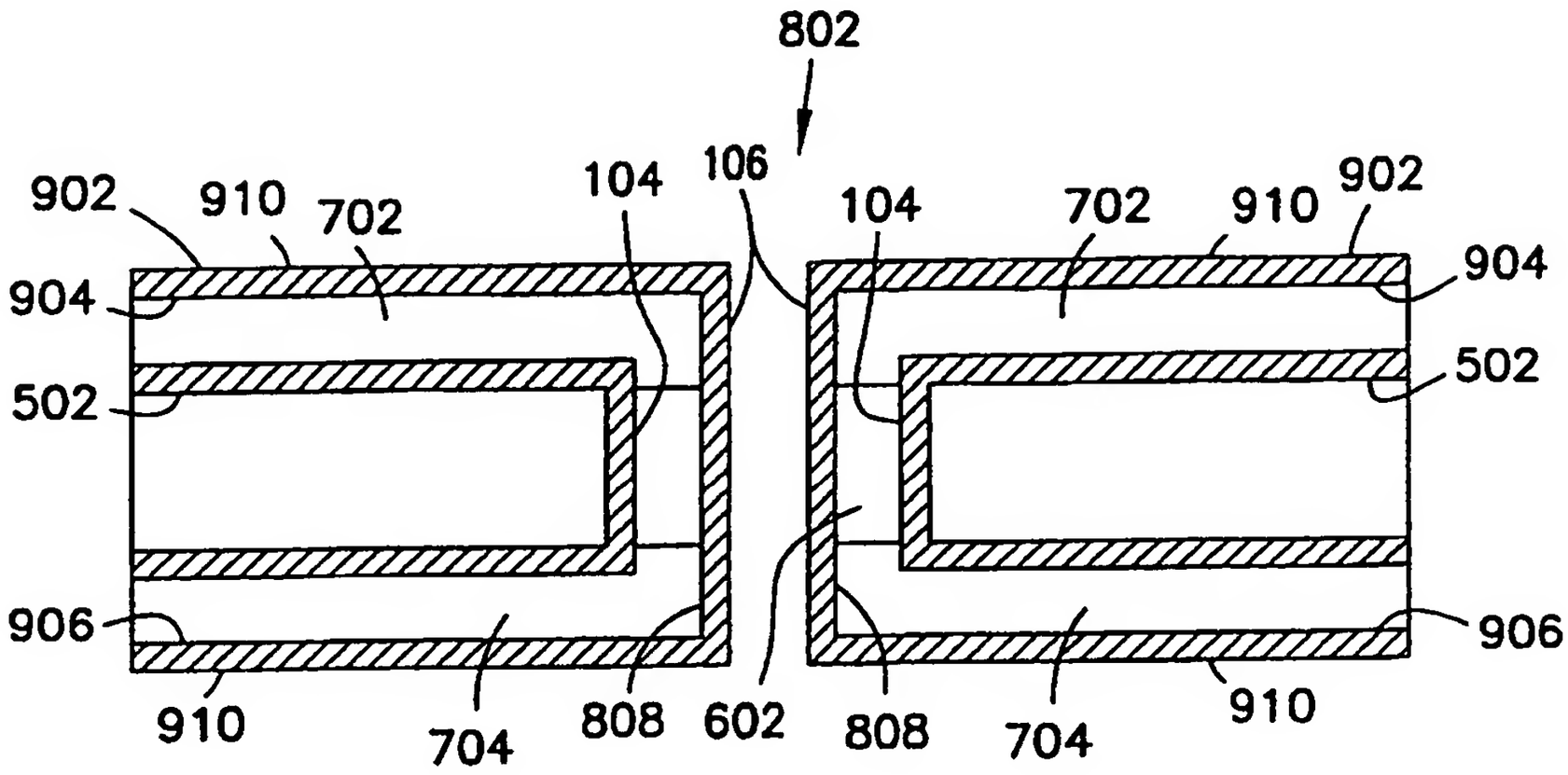
802
902
910
702
104
106
104
702
910
902
904
904
502
502
906
906
910
704
808
602
808
704
910

FIG. 10

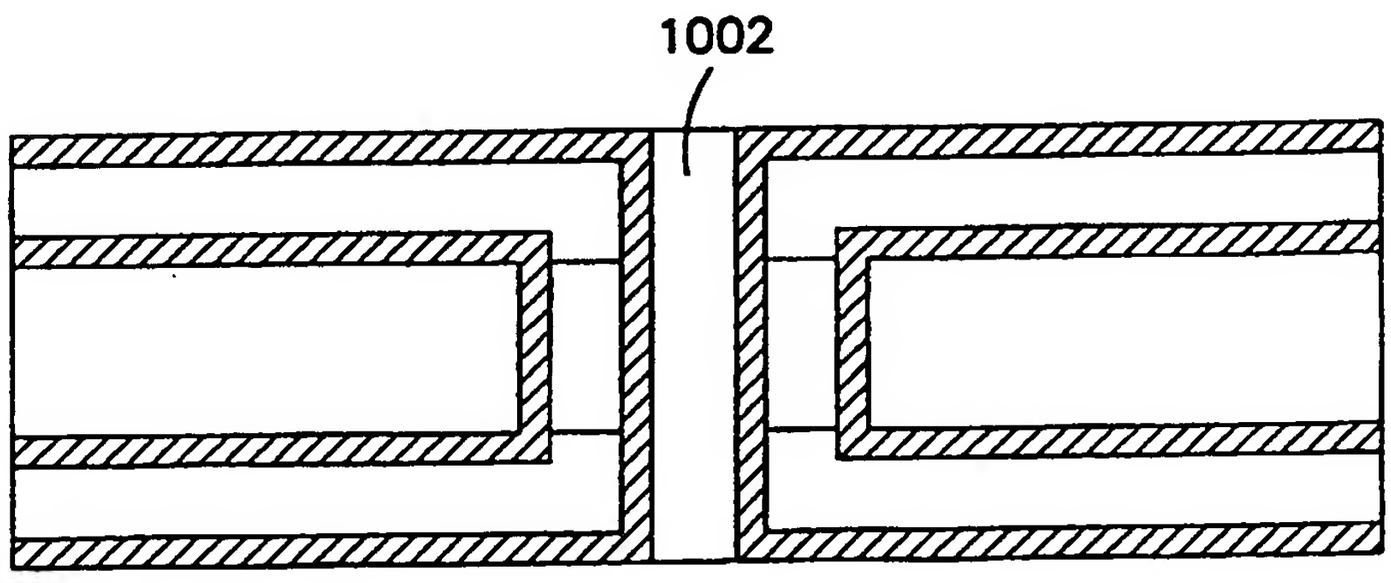
1002

FIG. 11

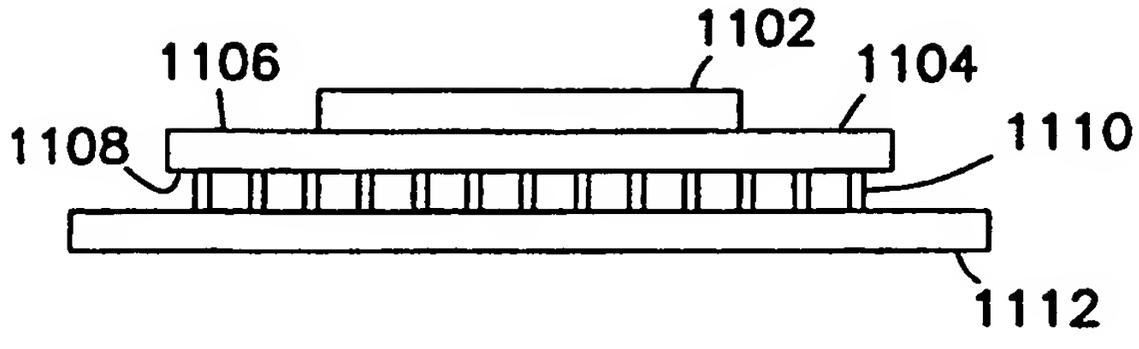
1102
1106
1104
1108
1110
1112

FIG. 12

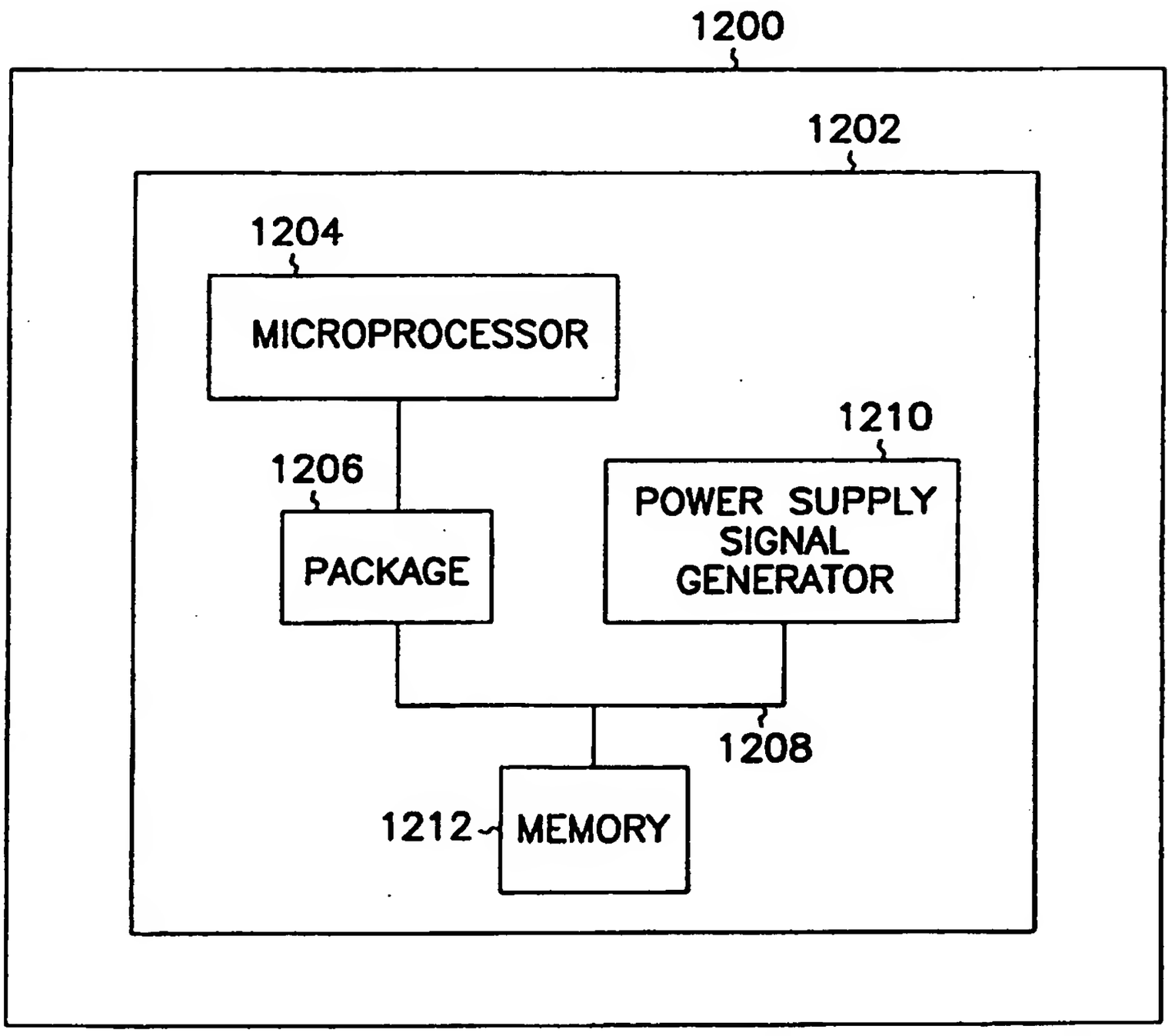
1200
1202
1204
MICROPROCESSOR
1210
1206
POWER SUPPLY
SIGNAL
GENERATOR
PACKAGE
1208
1212
MEMORY

FIG. 13